Aurora 8B/10B IP core
by ALSE

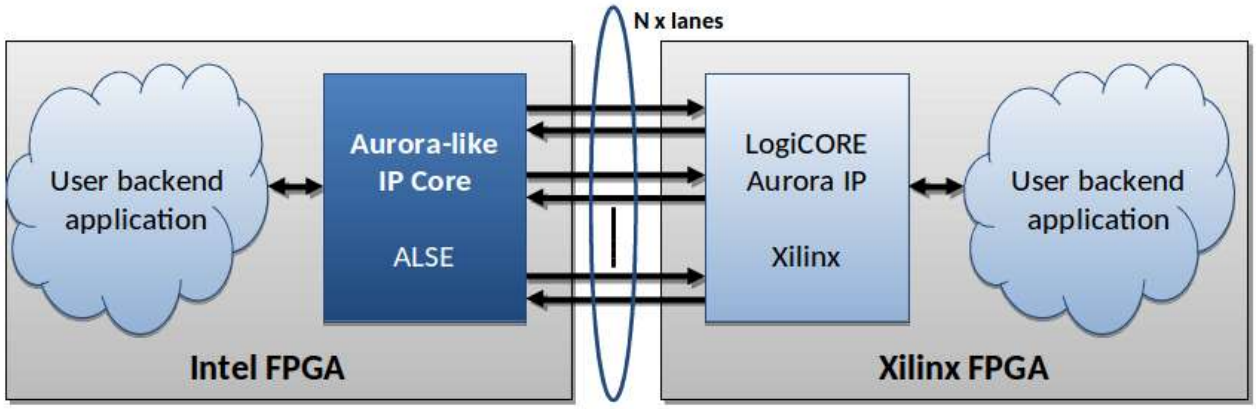
Advanced Logic Synthesis for Electronics

Introduction

Aurora 8B/10B is a public and lightweight protocol suitable for chip-to-chip, board-to-board and backplane communication using high speed transceivers. The ALSE Aurora 8B/10B IP core targets many FPGAs (Intel, Lattice, Microchip), and is compatible and fully interoperable with the Xilinx LogiCORE Aurora 8B/10B IP.

This IP core provides an efficient way to interconnect FPGAs from the same vendor or from different vendors (and even ASICs) using the public Aurora 8B/10B protocol. A common use case is to connect a Xilinx FPGA to an FPGA from another vendor.

Deliverables include a sophisticated HDL simulation environment for seamless development, verification and integration in the final application.



Features

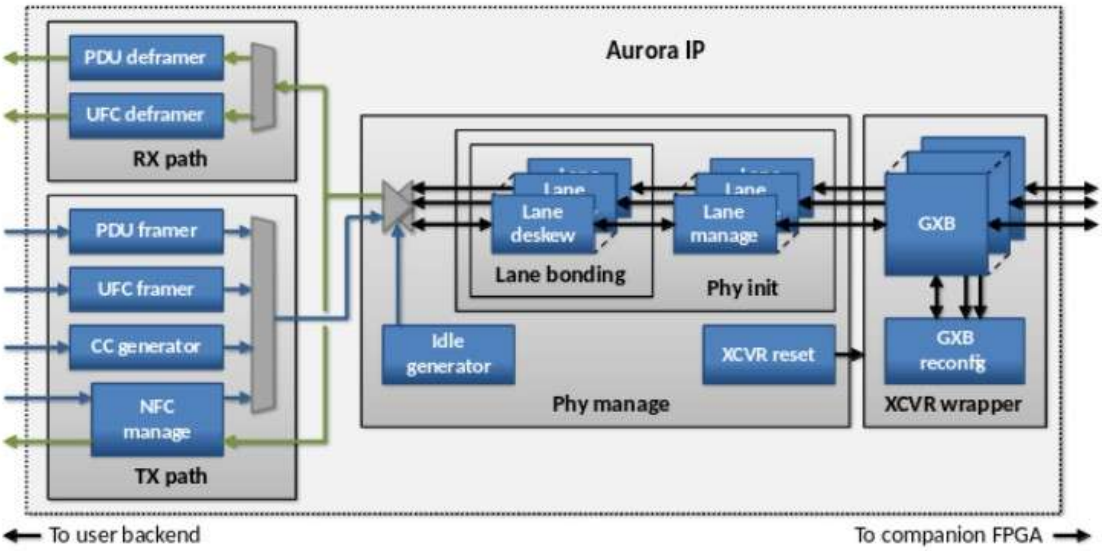
- Fully compatible with the standard Xilinx Aurora 8B/10B protocol
- Up to 16 Transceiver (XCVR) physical lanes
- Link Rate up to Device maximum XCVR Rate (e.g Cyclone V = 6.6 Gbps)
- Full Duplex and Simplex Tx operations supported
- 8B/10B encoding (please contact ALSE if you are interested by the Aurora 64B/66B IP core)
- Framing and Streaming interface
- User Flow Control (UFC)
- Native Flow Control (NFC, immediate/completion modes)
- Additional CRC for PDU Frames
- Clock compensation Sequence Generation
- Per lane polarity inversion, skew compensation
- Avalon-ST / AXI like Streaming user interfaces
- Provided with Hardware Reference designs, QIP files, SDC constraints

Examples of available Reference Designs

- ALSE Cyclone V Clovis/AVDB board ↔ Xilinx Virtex6 ML605 or Xilinx Virtex7 VC707 : 1 lane @ 3.125Gbps
- ReflexCES Intel Arria 10 Attila board ↔ Xilinx Virtex7 VC707 : 1 lane @ 6.25Gbps
- ReflexCES Intel Arria 10 Achilles board ↔ Arria 10 Attila Board : 4 lanes @ 6.25Gbps (Intel-FPGAs on both sides)
- Microchip Polarfire Dev kit ↔ VC 707 @ 5Gbps
- Lattice Certus Pro Nx board ↔ VC 707 @ 5Gbps
- etc …

Please note that ALSE can potentially build a demonstration on any suitable board within a short delay.

Block diagram



IP Resource utilization examples

Intel FPGA Device	XCVR Lanes	Framing / Streaming	Total User Data Path (Data Width per Lane)	ALMs	Memory Blocks (Memory Bits)
Cyclone V	1	Framing	16bits (16bits)	~780	2 x M10Ks (4096)
	1	Framing	16bits (16bits)	~930	2 x M10Ks (4096)
	1	Streaming	32bits (32bits)	~710	2 x M10Ks (4096)
	1	Streaming	32bits (32bits)	~750	2 x M10Ks (4096)
	4	Framing	128bits (32bits)	~2930	10 x M10Ks (77824)
	4	Streaming	128bits (32bits)	~1750	10 x M10Ks (77824)
Stratix V	1	Framing	32bits (32bits)	~1080	4 x M10Ks (36864)
	4	Framing	128bits (32bits)	~3100	8 x M10Ks (110592)
	4	Streaming	128bits (32bits)	~1950	8 x M10Ks (110592)
Arria 10	1	Framing	32bits (32bits)	~520	0 x M10Ks (0)
	4	Framing	128bits (32bits)	~2280	4 x M10Ks (73728)
	4	Streaming	128bits (32bits)	~1200	4 x M20Ks (73728)

Note: the numbers above include the transceiver logic.
Contact ALSE for getting implementation results on any other FPGA device family, or with specific modes (Simplex Tx, CRC).

Deliverables and Licensing Schemes

HDL Simulation Environment

- Pre-compiled simulations libraries
- Testbench and Simulation scripts

Complete User's Guide

SDC Constraints, QIP integration file

Hardware Tester Reference Design

Various licensing schemes

- Encrypted RTL
  - Timed or Untimed
  - Node Locked or Floating
  - Single or Multi-projects
- Source code RTL
- Netlist (per project or for multiple projects)

Contact :

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